WHAT IS CLAIMED IS:

1. An amplifier circuit comprising:

a cascode stage including a cascode transistor, the cascode transistor having a control terminal and first and second terminals, wherein the second terminal has an associated first voltage when the circuit is operating; and

a first differential stage having a first input coupled to the first terminal of the cascode transistor and a second input coupled to a node having an associated voltage approximately equal to the first voltage on the second terminal of the cascode transistor when the circuit is operating,

wherein a voltage difference between the first and second terminals of the cascode transistor is controlled by a voltage difference between the first input and second input of the first differential stage.

2. The amplifier circuit of claim 1 wherein the second input of the first differential stage is coupled to the second terminal of the cascode transistor.

3. The amplifier circuit of claim 1 wherein the cascode stage further comprises a second transistor having a control terminal and first and second terminals, wherein the control terminal of the second transistor is coupled to the control terminal of the cascode transistor and the second terminal of the second transistor is coupled to the second input of the first differential stage.

4. The amplifier circuit of claim 1 wherein the first differential stage has an offset voltage, the offset voltage being sufficient for biasing the first cascode transistor in the saturation region of operation.

5. The amplifier circuit of claim 4 wherein the first differential stage comprises first and second input transistors, the first and second input transistors having different characteristics so that the first differential stage generates an offset voltage.

6. The amplifier circuit of claim 5 wherein the first differential stage comprises first and second input transistors having different width to length ratios, and in accordance therewith, the first differential stage generates the offset voltage.

7. The amplifier circuit of claim 4 wherein the first differential stage comprises first and second input transistors, and wherein at least one of the first and second input transistors is coupled to a resistor so that the first differential stage generates an offset voltage.

8. The amplifier circuit of claim 3 further comprising a second differential stage having a first input coupled to a first terminal of the second transistor, a second input coupled to the second terminal of the cascode transistor, and an output coupled to the cascode stage for controlling the current in the cascode transistor and second transistor.

9. The amplifier circuit of claim 8 wherein the second differential stage includes an offset voltage to maintain the first terminal of the second transistor at an approximately fixed voltage above the second terminal of the cascode transistor.

10. The amplifier circuit of claim 8 wherein the first differential stage has a first offset voltage and the second differential stage includes a second offset voltage, wherein the first and second offset voltages are approximately matched to bias the first cascode transistor and the second transistor on the edge of the saturation region of operation.

11. The amplifier circuit of claim 1 wherein said amplifier comprises bipolar, MOS, or BiCMOS transistors.

12. An amplifier circuit comprising:

a cascode stage including first and second cascode transistors, the first and second cascode transistor having gates coupled to a first bias voltage; and

a first differential stage having a first input coupled to a drain terminal of the first cascode transistor, and a second input coupled to a source terminal of the second cascode transistor;

wherein the first differential stage includes a designed-in offset voltage.

13. The amplifier circuit of claim 12 wherein the amplifier further comprises first and second input transistors having control terminals to receive an input voltage, and in accordance therewith, generate a differential current in the cascode stage.

14. The amplifier circuit of claim 13 wherein the differential current is coupled to a source terminal of the first cascode transistor and the source terminal of the second cascode transistor.

15. The amplifier circuit of claim 12 wherein the cascode stage is connected in a folded cascode configuration.

16. The amplifier circuit of claim 12 wherein the offset voltage is greater than the voltage required to maintain the first cascode transistor in the saturation region of operation.

17. The amplifier circuit of claim 12 wherein differential stage includes first and second input transistors that have different width to length ratios to produce the offset voltage.

18. The amplifier circuit of claim 12 further comprising a second differential stage having a first input coupled to the drain terminal of the first cascode transistor, a second input coupled to the source terminal of the second cascode transistor, and an output.

19. The amplifier circuit of claim 18 wherein the second differential stage includes a designed-in offset voltage.

20. The amplifier circuit of claim 18 wherein the first differential stage and the second differential stage comprise opposite polarity devices.

21. The amplifier circuit of claim 18 further comprising first and second level shift circuits coupled to first and second inputs of the second differential stage.

22. The amplifier circuit of claim 18 further comprising a first output transistor having a control terminal coupled to an output of the first differential stage and a second output transistor having a control terminal coupled to the output of the second differential stage.

23. An amplifier circuit comprising:

a differential stage; and

a voltage dependent load coupled to an output node of the differential stage, wherein a voltage on the output node changes from a first voltage to a second voltage more positive than the first voltage,

wherein the gain of the differential stage increases as the voltage on the differential stage output node increases from the first voltage, reaches a maximum when the voltage on the differential output node is in a first voltage range between the first voltage and second voltage, and decreases as the voltage on the differential output node increases toward the second voltage.

24. The amplifier circuit of claim 23 wherein the voltage dependent load comprises a common gate stage coupled to the output of the differential stage.

25. The amplifier circuit of claim 24 wherein the differential stage comprises first and second input transistors.

26. The amplifier circuit of claim 25 wherein the differential stage further comprises a current mirror.

27. The amplifier circuit of claim 24 further comprising:

a first output transistor having a control terminal coupled to an output of the common gate stage; and

a second output transistor having a control terminal coupled to the output of the differential stage,

wherein the first and second output transistors are opposite polarity device types.

28. The amplifier circuit of claim 27 wherein the common gate stage comprises a NMOS transistor having a source coupled to the output of the differential stage, a drain coupled to a gate of the first output transistor, and a gate coupled to receive a bias voltage.

29. The amplifier circuit of claim 27 wherein the first output transistor is a PMOS transistor and the second output transistor is an NMOS transistor.

30. The amplifier circuit of claim 27 wherein the differential stage includes a first bias current, the current mirror comprises first and second transistors coupled

to receive the first bias current, and the common gate stage includes a second bias current, wherein the first transistor is sized to receive a first portion of the first bias current, and the second transistor is sized to receive a second portion of the first bias current in addition to the second bias current of the common gate stage, and wherein the gain of the differential stage changes in accordance with the input impedance of the common gate stage and the output impedance of at least one of the differential stage input transistors.

31. An amplifier circuit comprising:

a cascode stage including a cascode transistor, the cascode transistor having a control terminal and first and second terminals, wherein the second terminal has an associated first voltage when the circuit is operating;

a first differential stage having a first input coupled to the first terminal of the cascode transistor, a second input coupled to a node having an associated voltage approximately equal to the first voltage on the second terminal of the cascode transistor when the circuit is operating, and an output;

a common gate stage having an input coupled to the output of the first differential stage; and

an output stage including first and second output transistors, wherein at least one of the first and second output transistors includes a control terminal coupled to the output of the first differential stage.

32. The amplifier circuit of claim 31 wherein the second input of the first differential stage is coupled to the second terminal of the cascode transistor.

33. The amplifier circuit of claim 31 wherein the cascode stage further comprises a second transistor having a control terminal and first and second terminals, wherein the control terminal of the second transistor is coupled to the control terminal of the cascode transistor and the second terminal of the second transistor is coupled to the second input of the first differential stage.

34. The amplifier circuit of claim 31 wherein the cascode transistor comprises a PMOS or an NMOS transistor.

35. The amplifier circuit of claim 31 wherein first differential stage includes an offset voltage sufficient for biasing the cascode transistor in the saturation region of operation.

36. The amplifier circuit of claim 35 wherein first differential stage includes first and second input transistors that have different width to length ratios to produce the offset voltage.

37. The amplifier circuit of claim 31 wherein the common gate stage comprises a transistor having a source coupled to the output of the first differential stage and a gate coupled to a bias voltage.

38. The amplifier circuit of claim 31 wherein a control terminal of the first output transistor is coupled to an output of the common gate stage and a control terminal of the second output transistor is coupled to the output of the first differential stage.

39. The amplifier circuit of claim 31 wherein the cascode stage is connected in a folded cascode configuration.

40. The amplifier circuit of claim 31 further comprising at least one feed forward circuit.

41. The amplifier circuit of claim 40 wherein the feed forward circuit is coupled between the cascode stage and the output of the first differential stage.

42. The amplifier circuit of claim 40 wherein the feed forward circuit is coupled between the cascode stage and an output of the common gate stage.

43. A current mirror comprising:

a first transistor having a current input terminal, a current output terminal, and a control terminal;

a second transistor having a current input terminal, a current output terminal, and a control terminal, wherein the current input terminal of the second transistor is coupled to the current output terminal of the first transistor;

a third transistor having a current input terminal, a current output terminal, and a control terminal, wherein the control terminal of the third transistor is coupled to the control terminal of the first transistor;

a fourth transistor having a current input terminal, a current output terminal, and a control terminal, wherein control terminal of the fourth transistor is coupled to the

control terminal of the second transistor and the current input terminal of the fourth transistor is coupled to the current output terminal of the third transistor; and

a differential amplifier having a first input coupled to the current input terminal of the first transistor, a second input coupled to a node having an associated voltage approximately equal to the voltage on the current output terminal of the third transistor, and an output coupled to the control terminals of the second and fourth transistors.

44. The current mirror of claim 43 wherein the differential amplifier includes an offset voltage for the biasing the first transistor on the edge of the saturation region of operation.

45. The current mirror of claim 43 wherein the differential amplifier comprises first and second differential input transistors.

46. The amplifier circuit of claim 45 wherein the first and second differential input transistors are MOS transistors having different width to length ratios to produce the offset voltage.

47. The current mirror of claim 45 wherein the first differential input transistor is coupled to a resistor to produce the offset voltage.

48. The current mirror of claim 43 wherein the second input of the differential amplifier is coupled to the current output terminal of the third transistor.

49. The current mirror of claim 43 further comprising a bias circuit including a fifth transistor having a control terminal coupled to the control terminals of the first and third transistors, wherein the second input of the differential amplifier is coupled to a current output terminal of the fifth transistor.

50. The current mirror of claim 43 wherein the first, second, third, and fourth transistors are NMOS or PMOS transistors, and the current input terminals are drains, the current output terminals are sources, and the control terminals are gates.

51. The current mirror of claim 43 wherein the first, second, third, and fourth transistors are NPN or PNP transistors, and the current input terminals are collectors, the current output terminals are emitters, and the control terminals are bases.